

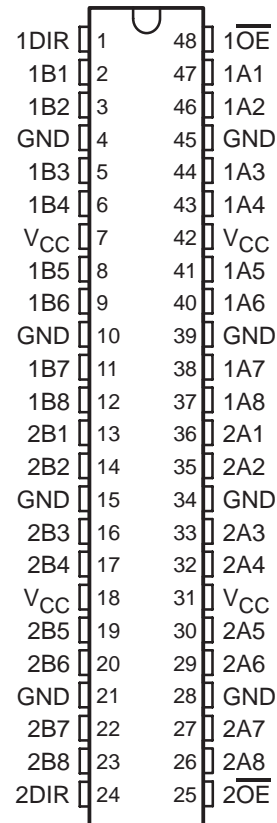
# SN74LVTH16245A-Q1

## 3.3-V ABT 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS772C – JUNE 2004 – REVISED JANUARY 2008

- Qualified for Automotive Applications
- Member of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Supports Unregulated Battery Operation Down To 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17

DGG OR DL PACKAGE  
(TOP VIEW)



### description/ordering information

The SN74LVTH16245A is a 16-bit (dual-octal) noninverting 3-state transceiver designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the devices so that the buses are isolated.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with bus-hold circuitry is not recommended.



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## 3.3-V ABT 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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### description/ordering information (continued)

When  $V_{CC}$  is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  shall be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

### ORDERING INFORMATION†

TA	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SSOP – DL	Tape and reel	CLVTH16245AQDLRQ1§	LH16245AQ1
	TSSOP – DGG	Tape and reel	CLVTH16245AQDGGRQ1	LH16245AQ1

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

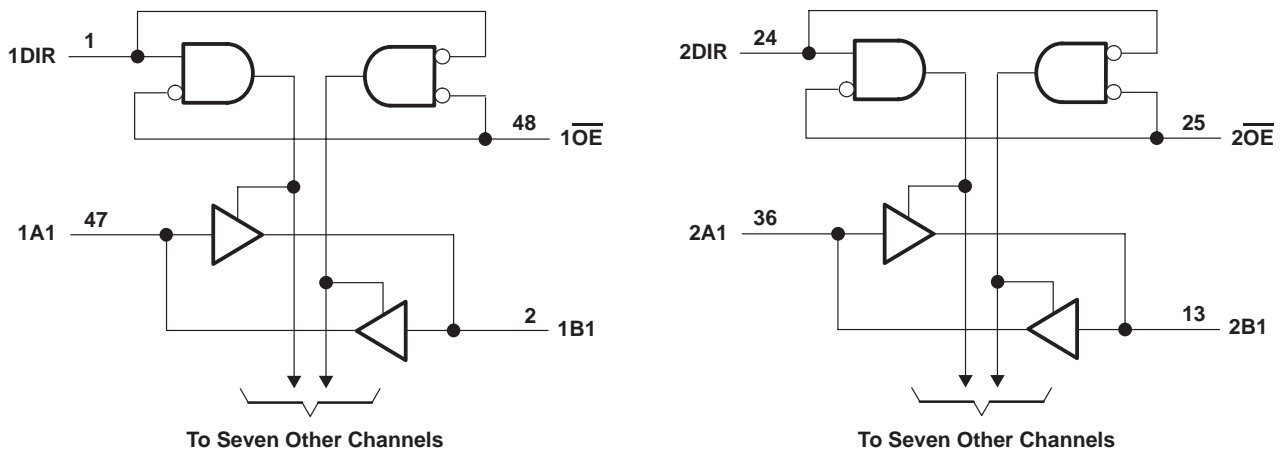
‡ Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

§ Product Preview

### FUNCTION TABLE (each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

### logic diagram (positive logic)



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## 3.3-V ABT 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_{OL}$ .....	96 mA
Current into any output in the high state, $I_{OH}$ (see Note 2) .....	48 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package .....	70°C/W
DL package .....	63°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 4)

		SN74LVTH16245AQ				UNIT
		$T_A = -40^\circ\text{C TO } 125^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 85^\circ\text{C}$		
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		24		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu\text{s/V}$

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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## 3.3-V ABT 16-BIT BUS TRANSCEIVER

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN74LVTH16245AQ						UNIT		
			-40°C TO 125°C			-40°C TO 85°C					
			MIN	TYP†	MAX	MIN	TYP†	MAX			
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$		-1.2			-1.2			V		
$V_{OH}$	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC} - 0.2$			$V_{CC} - 0.2$			V		
	$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$		2.4			2.4					
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2								
$I_{OH} = -32\text{ mA}$					2						
$V_{OL}$	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$				0.2			V		
		$I_{OL} = 24\text{ mA}$				0.5					
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$				0.4					
		$I_{OL} = 32\text{ mA}$				0.5					
		$I_{OL} = 64\text{ mA}$				0.55					
$I_I$	Control inputs	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND		$\pm 1$			$\pm 1$			$\mu\text{A}$	
		$V_{CC} = 0$ or $3.6\text{ V}$ , $V_I = 5.5\text{ V}$		10			10				
	A or B ports‡	$V_{CC} = 3.6\text{ V}$	$V_I = 5.5\text{ V}$		20			20			
			$V_I = V_{CC}$		5			1			
		$V_I = 0$		-5			-5				
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to $4.5\text{ V}$					$\pm 100$			$\mu\text{A}$		
$I_{I(\text{hold})}$	A or B ports	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$		75			75			$\mu\text{A}$
			$V_I = 2\text{ V}$		-75			-75			
		$V_{CC} = 3.6\text{ V}\S$ , $V_I = 0\text{ V to }3.6\text{ V}$					500 -750			$\mu\text{A}$	
$I_{OZPU}$	$V_{CC} = 0$ to $1.5\text{ V}$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $OE = \text{don't care}$		$\pm 100$			$\pm 100$			$\mu\text{A}$		
$I_{OZPD}$	$V_{CC} = 1.5\text{ V to }0$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $OE = \text{don't care}$		$\pm 100$			$\pm 100$			$\mu\text{A}$		
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND	Outputs high		0.19			0.19			mA	
		Outputs low		5			5				
		Outputs disabled		0.19			0.19				
$\Delta I_{CC}\P$	$V_{CC} = 3\text{ V to }3.6$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND		0.2			0.2			mA		
$C_i$	$V_I = 3\text{ V or }0$		4			4			pF		
$C_{io}$	$V_O = 3\text{ V or }0$		10			10			pF		

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Unused pins at  $V_{CC}$  or GND

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.



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**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

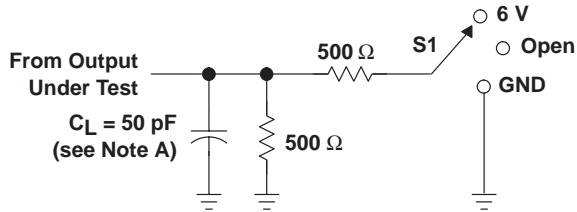
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVTH16245AQ								UNIT	
			-40°C TO 125°C				-40°C TO 85°C					
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
$t_{PLH}$	A or B	B or A	0.5	4.5	4.6		1.5	2.3	3.3	3.7		ns
$t_{PHL}$			0.5	4.4	3.9		1.3	2.1	3.3	3.5		
$t_{PZH}$	$\overline{OE}$	A or B	0.5	6.5	6.6		1.5	2.8	4.5	5.3		ns
$t_{PZL}$			0.5	5.4	6.2		1.6	2.9	4.6	5.2		
$t_{PHZ}$	$\overline{OE}$	A or B	1	6.8	7		2.3	3.7	5.1	5.5		ns
$t_{PLZ}$			1	6.2	6.3		2.2	3.5	5.1	5.4		
$t_{sk(o)}$									0.5	0.5	ns	

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

**SN74LVTH16245A-Q1**  
**3.3-V ABT 16-BIT BUS TRANSCEIVER**  
**WITH 3-STATE OUTPUTS**

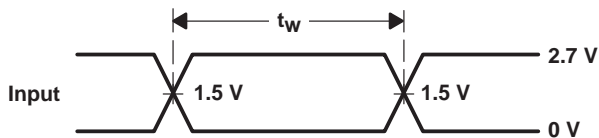
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**PARAMETER MEASUREMENT INFORMATION**

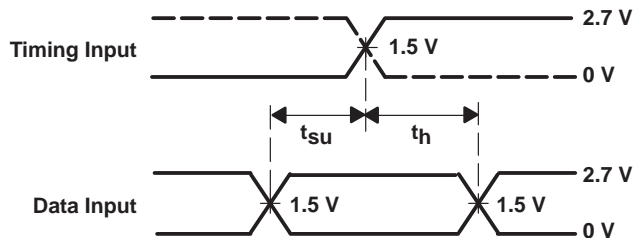


**LOAD CIRCUIT**

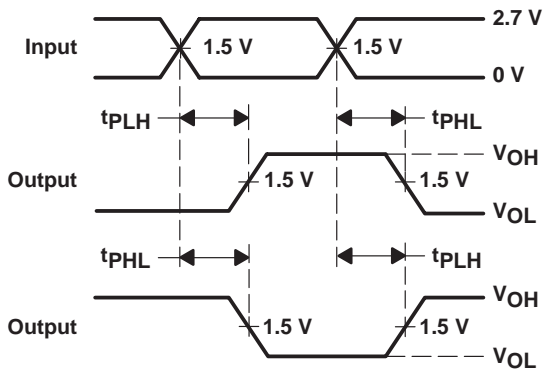
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



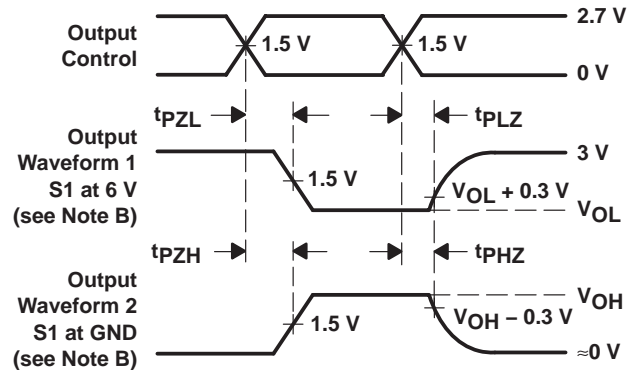
**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**  
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**  
**LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CLVTH16245AQDGGRRQ1	ACTIVE	TSSOP	DGG	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN74LVTH16245A-Q1 :**

- Catalog: [SN74LVTH16245A](#)
- Enhanced Product: [SN74LVTH16245A-EP](#)
- Military: [SN54LVTH16245A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



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